UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,247	03/24/2004	Tadashi Matsuda	251007US2	4517

22850 7590 08/08/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,247	MATSUDA, TADASHI	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 12* is/are allowed.

6)☒ Claim(s) *1-4,13 and 14* is/are rejected.

7)☒ Claim(s) *5-10 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *March 24, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the papers filed on March 24, 2004.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claims 1-4, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 6,072,214 to Herzer et al. (Herzer).

With respect to independent claim 1, Herzer discloses a semiconductor device including a trench gate IGBT (see the entire patent, including the Fig. 5 disclosure), comprising: a first semiconductor layer 12 of a first (p) conductivity type; a second semiconductor layer 1 of a second (n) conductivity type which is formed on one surface of said first semiconductor layer; a base layer 2 of the first conductivity type which is formed in a surface portion of the second semiconductor layer; emitter layers 3 of the second conductivity type which are selectively formed in a surface portion of said base layer; a plurality of trenches 5 which extend through said emitter layers and said base

layer and are formed to a predetermined depth in the second semiconductor layer; gate electrodes 7 which are formed on gate insulating films 6 in the trenches; an emitter electrode 14 which is formed on said emitter layers and said base layer; a collector electrode 13 which is formed on the other surface of said first semiconductor layer; an auxiliary base layer 18 of the first conductivity type which is formed in an arbitrary region between two adjacent trenches and is insulated from said emitter electrode; and a carrier discharge electrode 19 which contacts a surface of said auxiliary base layer of the first conductivity type.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Herzer.

With respect to dependent claim 2, Herzer's device further comprises a MISFET including a channel region of the first conductivity type (i.e., a p-MISFET), wherein a source 18 of said MISFET is connected to said carrier discharge electrode 19 of the trench gate IGBT, and a drain 2 of said MISFET is connected to said emitter electrode 14 (via contact region 4) of the trench gate IGBT.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Herzer.

With respect to dependent claim 3, a gate electrode 6 of Herzer's MISFET is electrically connected to said gate electrode 6 of the trench gate IGBT (i.e., Herzer's MISFET and IGBT share gate electrode 6).

Claim 3 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Herzer.

With respect to dependent claim 4, Herzer's MISFET is mounted in the same package as a package of the trench gate IGBT (because they are integrated).

Claim 4 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Herzer.

With respect to independent claim 13, Herzer discloses a semiconductor device including a trench gate IGBT (see the entire patent, including the Fig. 5 disclosure), comprising: a trench gate IGBT having a first semiconductor layer 12 of a first (p) conductivity type; a second semiconductor layer 1 of a second (n) conductivity type which is formed on one surface of the first semiconductor layer; a base layer 2 of the first conductivity type which is formed in a surface portion of the second semiconductor layer; emitter layers 3 of the second conductivity type which are selectively formed in a surface portion of the base layer; a plurality of trenches 5 which extend through the emitter layers and the base layer and are formed to a predetermined depth in the second semiconductor layer; gate electrodes 7 which are formed on gate insulating films 6 in the trenches; an emitter electrode 14 which is formed on the emitter layers and the base layer; a collector electrode 13 which is formed on the other surface of the first semiconductor layer; an auxiliary base layer 18 of the first conductivity type which is formed in an arbitrary region between two adjacent trenches, and a carrier discharge electrode 19 which contacts a surface of the auxiliary base layer of the first conductivity type; and a MISFET which includes a channel region of the first conductivity type (i.e., a p-MISFET), and includes a source 18 connected to the carrier discharge electrode 19 of the trench gate IGBT, a drain 2 connected to the emitter electrode 14 (via contact region 4) of the trench gate IGBT, and a gate electrode 6 electrically connected to the gate electrode of the trench gate IGBT (i.e., the MISFET and IGBT share gate electrode 6).

Claim 13 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Herzer.

With respect to dependent claim 14, Herzer's MISFET is mounted in the same package as a package of the trench gate IGBT (because they are integrated).

Claim 4 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Herzer.

Claims 5-10 and 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11 and 12 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable semiconductor device including a trench gate IGBT taken as a whole, including the carrier discharge electrode.

United States Patent Application Publication 2005/0156201 is related to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner